Electronic Version
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# Active ESD Shunt with Transistor Feedback to Reduce Latch-Up Susceptibility

## Abstract

A VDD-to-VSS clamp shunts current from a power node to a ground node within an integrated circuit chip when an electrostatic-discharges (ESD) event occurs. A resistor and capacitor in series between power and ground generates a low voltage on a trigger node between the resistor and capacitor when an ESD event occurs. A p-channel transistor with its gate driven by the trigger node turns on, driving a gate node high. The gate node is the gate of an n-channel shunt transistor that shunts ESD current from power to ground. A p-channel feedback transistor terminates the ESD shunt current. The p-channel feedback transistor is connected between power and the trigger node, in parallel with the resistor, and has the gate node as its gate. When a latch up trigger occurs, such as electron injection, voltage drops across an N-well of the resistor is prevented by the parallel p-channel feedback transistor.